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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,063	01/03/2002	Brian Schott	06666-097001/USC-2958	5752

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SCOTT C. HARRIS
Fish & Richardson P.C.
Suite 500
4350 La Jolla Village Drive
San Diego, CA 92122

EXAMINER

DINH, PAUL

ART UNIT PAPER NUMBER

2825

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/038,063

Applicant(s)

SCHOTT ET AL.

Examiner

Paul Dinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) 1-29 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 30-32 and 34-42 is/are rejected.
- 7) ☒ Claim(s) 33, 43 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 January 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input checked="" type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/3/02 and 5/6/03</u> | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

This is a response to the applicant election of claims 30-43 without traverse.

Applicant request for the non-elected claims 1-29 as withdrawn from consideration is acknowledged. However, the applicant is advised that cancellation of the non-elected claims 1-29 is required. The restriction is final.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Claims 38-39 recite a memory (SRAM) connected to each processing elements; therefore, this feature must be clearly shown in the drawings or this feature canceled from the claims.

Claim Objections

In claim 1 and claim 43, "first" and "second" should be checked and added accordingly for clarification, correctness, and antecedent basis; for examples; claim 1 should recite "a first ring", "a first chain", "the first chain", "a first control element", "data entering the first ring" to distinguish from claim 43 that should recite "a second chain" (lines 5-6), "the second chain" (lines 7-8) "a second control element" (line 9), "data entering the second ring" (line 11), etc.

In claim 42, "the interfaces device" should be changed to "the interface device"

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 30-32, 35-36, 38-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Casselman (USP 5802290 from IDS filed 1/3/02) who discloses an apparatus comprising:

(Claim 30)

a plurality adaptive computing elements (*adaptive computing elements are virtual computers (fig 2-3, 12, 16) of the virtual network (fig 1)*) connected in a ring configuration (col 8 lines 22-23), including

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plurality of processing elements (*processing elements are, i.e., reconfigurable FPGA computation array 20 in fig 2, FPGAs 31-32 in fig 3, 5, 7, FPGA 202 in fig 12*) connected in a chain configuration and including a first processing element (FPGA 31) at first end of the chain and a second processing element (FPGA 32) at second end of the chain, and

a control element (*i.e., control element 21 in fig 2, 206 in fig 12, 14*) connected to the first processing element and the second processing element, and operative to manage data entering the ring;

a bus (bus 220 in fig 12, 15-16), and

an interface device (VME interface 216 in fig 12) connected between the control element and the bus.

(Claim 31) The apparatus of claim 30, wherein each of adaptive computing elements comprises an FPGA IC (abstract lines 11-13, col 2 lines 25-29).

(Claim 32) The apparatus of claim 30, wherein the ring includes two processing elements (FPGA 31, FPGA 32 in fig 3).

(Claim 35) The apparatus of claim 30, wherein the bus comprises a VME (Versa Module Europa) bus (see VME bus in fig 12, 15).

(Claim 36) The apparatus of claim 30, further comprising a host processor (*host processor in host computer 12 of fig 2-3, 5, 7, 602 of fig 16*) connected to the bus and operative to configure the adaptive computing elements.

(Claims 38-39) The apparatus of claim 30, further comprising an SRAM memory device connected to each of the processing elements (SRAM 49 in fig 3).

(Claim 40) The apparatus of claim 30, wherein the interface device is integrated in the control element (*see abstract lines 11-13, col 2 lines 25-29 that teaches each virtual computer (fig 2-3, 12) has an FPGA or an Array of FPGAs wherein the interface device (interfacing function/module/section) and the control (control function/module/section) element (shown as VME interface 216 and reconfigurable control 206 in fig 12) are programmed, configured, reconfigured and integrated.*

(Claim 41) The apparatus of claim 30, further comprising an integrated circuit (IC) including the processing elements and the control element (*see abstract lines 11-13, col 2 lines 25-29 that teaches each virtual computer (fig 2-3, 12) has an FPGA or an FPGA or an Array of FPGAs (IC)) wherein the processing (processing functions/modules/sections) elements (i.e., shown as reconfigurable FPGA computation array 20 and 200 in fig 2 and 12, respectively, FPGAs 31-32 in fig 3, 5, 7) and the control*

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(control function/module/section) element (i.e., shown as control element 21 in fig 2, 206 in fig 12, 14) are programmed, configured, reconfigured and integrated).

(Claim 42) The apparatus of claim 30, wherein the interface device comprises an FPGA

(Field Programmable Gate Array) integrated circuit *(see abstract lines 11-13, col 2 lines 25-29 that teaches each virtual computer (fig 2-3, 12) has an FPGA (integrated circuit) wherein the interface (interfacing function/module/section) device (shown as VME interface 216 in fig 12) is programmed, configured, reconfigured and integrated.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

(a) Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Casselman (USP 5802290) in view of Secila, III et al. (USP 5875313) and/or Maroney (USP 5925119) and/or Tseng (US patent Publication N. 2002/0152060)

Casselman discloses substantially all the elements in claim 34 except the PCI bus.

Secila discloses the PCI bus in col 5 line 60 to col 6 line 2;

Maroney discloses the PCI bus in col 5 lines 60-65 and col 11 lines 10-12; and

Tseng discloses the PCI bus in paragraph [0197].

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a PCI bus because PCI bus is a high performance bus and well known in the art (as taught by Secila) and/or because PCI bus is well known, preferred, available, industry standard, and capable of supporting high speed host interfaces (as taught by Maroney) and/or because PCI bus is available, standard, and fast (as taught by Tseng).

(b) Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Casselman (USP 5802290) in view of Rossi (USP 5663721) and/or Jolitz et al (USP 6173333).

Casselman discloses substantially all the elements in claim 37 except the ACS accelerator

Rossi discloses the ACS accelerator in fig 2; and

Jolitz discloses the ACS accelerator in fig 1.

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It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize an ACS accelerator because an ACS accelerator accelerates (speeds up) network transmission and communication as taught by Rossi and/or Jolitz.

Allowable Subject Matter

Claims 33 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 33 would be allowable because the prior art does not teach or suggest a crossbar data path connecting the control element to each of the two processing elements.

Claim 43 would be allowable because the prior art does not teach or suggest a second plurality of adaptive computer elements connected in a second ring configuration with all the elements, configuration, paths, and connections in claim 43.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh

Patent Examiner

Paul Dinh
7/22/04